

FORM PTO-892 (REV. 2-92) US DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE ATTACHMENT SERIAL NO. **GROUP ART UNIT** TO PAPER NUMBER 09/389,567 2183 6 NOTICE OF REFERENCES CITED APPLICANT(S) Ross et al. **U.S. PATENT DOCUMENTS** DOCUMENT NO. DATE NAME **CLASS SUBCLASS** Α 6,215,327 04-10-2001 Lyke 326 41 В 5,621,337 04-15-1997 Childs 46 326 C | 5,444,393 08-22-1995 Yoshimori et al. 326 38 D 5,389,838 02-14-1995 Orengo 326 93 4,786,829 11-22-1988 Letcher 326 46 F 4,706,217 11-10-1987 Shimizu et al. 326 46 G 4,331,893 05-25-1982 Conners 326 46 H 3,328,767 06-27-1967 Ottaway 712 221 Ι J K FOREIGN PATENT DOCUMENTS SUB-CLASS DOCUMENT NO. DATE COUNTRY CLASS NAME L Μ Ν 0 P Q OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.) Ohta et al., New FPGA Architecture for Bit-Serial Pipeline Datapath, Proceedings of the IEEE Symposium on FPGAs for R Custom Computing Machines, pp. 58-67, April 15-17, 1998. S Т U EXAMINER DATE Richard Ellis April 29, 2003 A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)